ISSI DDR3 SDRAM Layout Guidelines

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Introduction

This is a general PCB layout guideline for ISSI DDR3 SDRAM, especially targeting point to point applications. DDR3 is an evolutionary transition from previous memory generations of DDR2 products which increases clock frequencies and bandwidth with on the fly calibration to adjust for voltage and temperature variations to maintain stable Output drive characteristics, On-Die termination (ODT) with dynamic control and additional advanced features that are ideally suited for point to point applications. In DDR3 board designs controller manufacturers may require special or additional guidelines in these cases ISSI recommends the controller guidelines be applied first and confirmed to ISSI component specifications are not violated.

PCB Layout Guidelines

FR-4 is commonly used for the dielectric material. Thickness and trace widths should be adjusted to match the desired impedance. Trace lengths are also important and their performance impact should be confirmed in simulations for each of the critical clock and net groups. Generally, single impedances (CA, Control & DQ's) are 50Ω (+/- 10%) and differential impedances (Clocks, DQS's) are nominally 100Ω (+/- 10%) and are typically routed on inner layers if possible. In slower applications, crosstalk issues would be less and closer spacing may be allowed after careful simulation to evaluate the design rule changes. Minimum spacing guidelines in these examples are dependent on dielectric thickness, routing pitch and should be verified with simulations to reduce intranet/internet group coupling/crosstalk. All impedances should be verified and monitored for each layer to make sure they comply with design specifications.

Power Distribution

As clock frequencies increase power distribution networks (PDN) must be carefully controlled to insure adequate timing margin and noise immunity. This is especially critical in wide I/O designs where simultaneous switching of the outputs (SSO) is common. In this case power distribution networks can experience large peak current demands on Vddq and Vssq lines. If the power network isn't carefully designed, peak current demand (High Drive Strength) can negatively impact timing margins and in extreme cases cause power supply deficiencies. Supply and ground planes, routing and decoupling should be checked insure optimal voltage/current supply for DDR3 devices.

The following are general guidelines for PDN development in DDR3 board designs.

1. Solid Power and Ground planes should be used in DDR3 routing areas.
2. Place a 0.1uF cap and 0.01uF as close as possible for every VDDQ pin.
3. VTT decoupling should be as close to the components and pull-up resistors as possible.
4. Place a 0.1uF decoupling cap between VTT and VDD.
5. Low ESL decoupling capacitors should be used and routing should be carefully evaluated to minimize inductance.
6. Power connections from supply planes to vias for device pins or decoupling capacitors should be as short (<8 mils) and as wide as possible (trace widths should be the same or larger than the via size) to minimize trace impedance.

A hierarchical design approach is recommended in DDR3 board layout with differential clocks (CK/CK#) and Data Strobes (DQS/DQS#). Overall routing lengths for these signals (CK/CK# & DQS/DQS#) should be controlled / matched to within ±2 ps or a maximum of 10mils between true and compliment signals. Route the CK/CK# clocks and set as the target trace propagation delays for the DQ net group. Match the CK/CK# clock to within ±5 ps of all DQS/DQS#. DQ and DM net groups should be routed with their respective DQS/DQS# and DM on the same PCB layer and matched within ±10ps, maximum difference of 50mils. DQS/DQS# should be used as the target trace propagation delay for the associated Data and data mask signals.
Route the address/control signal group ideally on the same layer as the CK/CK# clocks, to within ±10 ps skew of the CK/CK# traces. Following table is a good example for baseline specifications at the beginning of a board design. Values in this table are general guidelines and should be confirmed with board simulations to verify design targets and operating margins.

Signals on Net	Maximum deviation of signal propagation difference.	Maximum deviation of trace length.
Between signals within byte group (DQS,DM,8bits of DQ)	±10ps	±1.270mm(50mil)
Between signals within address net. Between signals within commands net. Between one byte group and another byte group.	±50ps	±6.635mm(261mil)
Between CK and CK#. Between DQSn and DQS#n	±2 ps	±0.254mm (10mil)

Notes:

1. Minimum trace width is 0.13mm (5mil).
2. Intranet spacing, the distance between two adjacent traces within a net, is 8mil (depending on dielectric thickness)
3. Internet spacing, the distance between the two outermost signals of different signal group is 15mil. Same rule applies between one clock pair and another clock pair.
4. Differential clocks should be routed in parallel with short trace lengths.
5. Differential clocks must be routed on the same layer and placed on an internal layer minimize the noise.
6. Due to crosstalk and signal noise reduction keeping the trace lengths as short possible ISSI recommends less that 20mm.
7. Signals from the same net group should be routed on the same layer.
8. Signals from the same Byte group, such as DQS, DM and 8 bits of DQ, must be routed in the same layer

V_{REF} Control

V_{REF} should be designed to provide optimum noise margin in the system. V_{REF} levels must be carefully controlled and isolated from noise conditions to prevent potential timing errors which can reduce setup and hold time margins, increase jitter, and cause erratic memory bus behavior. V_{REF} is expected to track variations in V_{DDQ} and the peak to peak noise must remain within specification.

1. Place a 0.1uF capacitor between V_{REF} and V_{DDQ}
2. Place a 0.1uF capacitor between V_{REF} and V_{SSQ}
3. V_{REF} should have a minimum trace length to reduce inductance.
4. V_{REF} should have a wide trace. Min 20 mil is recommended.
5. V_{REF} should maintain a minimum of 25mil width and spacing from other signals to minimize coupling effects and ideally be isolated with adjacent ground traces.
6. Each V_{REF} source and destination should be decoupled with 0.1uF caps.

EMI and Termination.

The DDR3 SDRAM uses a programmable impedance output buffer. The output drive strength is calibrated during initialization, this feature minimizes any process variation present in the driver. To calibrate output driver impedance, RZQ needs to be located between the ZQ ball and VSSQ. The value of RZQ must be 240Ω ±1% and can't be shared. Each DDR3 should have its own RZQ. Drive strength is selected by programming value in the memory mode register 1 (MR1). The default strength is RZQ/6(=40Ω). In layout, the impedance for all single ended data groups is approximately 50Ω and differential signals are nominally 100Ω. Refer to the controller manufacturers design guideline for the any restrictions or recommendations.

LAND pattern

Follow IPC-SM-782A, keep size of land pattern to be equal to 80% of the ball size of BGA.

Please contact the ISSI Application Engineering team for any DDR3 product development questions.

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