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Designing with DrMOS
Part I: Concept and Features

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Introduction

The synchronous buck converter has become the ubiquitous standard in electronic equipment. While the basic topology is rather simple, implementation has been evolving over the years to meet ever increasing demand for higher efficiencies and power densities. Some of the major changes have been asymmetric differentiation of high side and low side MOSFETs, with the HS FET optimised for ultra fast switching and the LS FET optimised for minimum conduction losses, integration of Schottky structures into the body diode of the LS FET etc. Recently the popular SO-8 has given way to a variety of DFN and QFN packages which permit higher die sizes and better thermal interface within the same footprint. There is also a new class of power ICs which combine the PWM controller and the MOSFETs in one package to offer compact and efficient power conversion solutions. However the power ICs are somewhat limited in their scope since the controller can have a small, fixed feature set and output current is also limited by the package. The recent DrMOS power modules[(1)] are an excellent solution optimised for high frequency power conversion at high output currents.

A major issue in improving the performance of synchronous buck converters has been the unavoidable presence of interconnecting inductances and resistances in the power stage. Today's converters switch at frequencies of hundreds of kHz where even a few nanohenries of stray inductance can affect the performance. *Fig. 1* shows the sources of parasitic inductances in the input current loop of the synchronous buck converter. Most of them are due to bond wires, package pins and the minimal traces that are needed to connect different discrete packages. The gate loop inductances also contribute to slower switching, ringing, and in extreme cases shoot through conditions. With low voltage MOSFET $R_{DS(ON)}$ values approaching 1 mΩ, the combined resistance of bond wires, pins and short traces adds up to a significant number. DrMOS eliminates most of these unwanted parasitics by integrating the power train and the driver in the same package. The pinout is further optimised so that input bypass capacitors may be placed very close to package leads for low inductance routing.

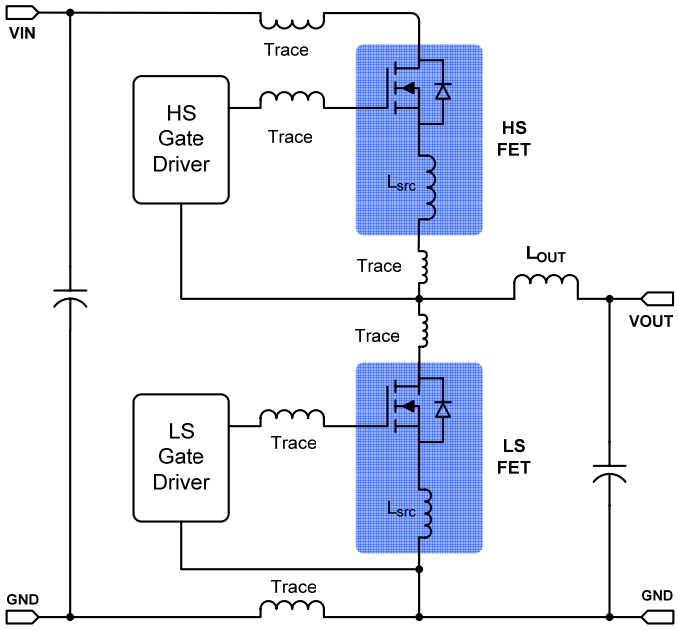

Fig. 1. Parasitic inductances in a synchronous buck circuit

The DrMOS Concept

DrMOS is an obvious acronym for Driver and MOSFET Module. It is a high efficiency synchronous buck power module consisting of two asymmetrical MOSFETs and an integrated driver. DrMOS was initially defined by Intel in 2004 as an 8x8 56 pin QFN package for the power hungry VRM modules[(2)]. The driver section had a fairly wide menu of features including user defined drive voltages. However it wasn't well received in the PC market mainly because of cost and complexity. A smaller version in QFN 6x6 package with 40 leads and fewer logic features was proposed by Intel in 2007 under DrMOS Specification Rev 3.0[(3)]. This new version is simpler and gaining wider acceptance among desktop, server, graphics card, gaming console and telecom power convertor designers.

One of main benefits of DrMOS concept is that the driver and MOSFETs can be closely matched as a single unit for optimum switching performance. A number of well thought features are provided in the driver section making the DrMOS a highly versatile power module. Boot supply diode is integrated in the driver. The low side MOSFET can be driven into diode emulation mode to provide asynchronous operation when required. The PWM input is tri-state compatible which allows both power MOSFETs to be turned off. The basic block diagram of the DrMOS module is shown in *Fig. 2*.

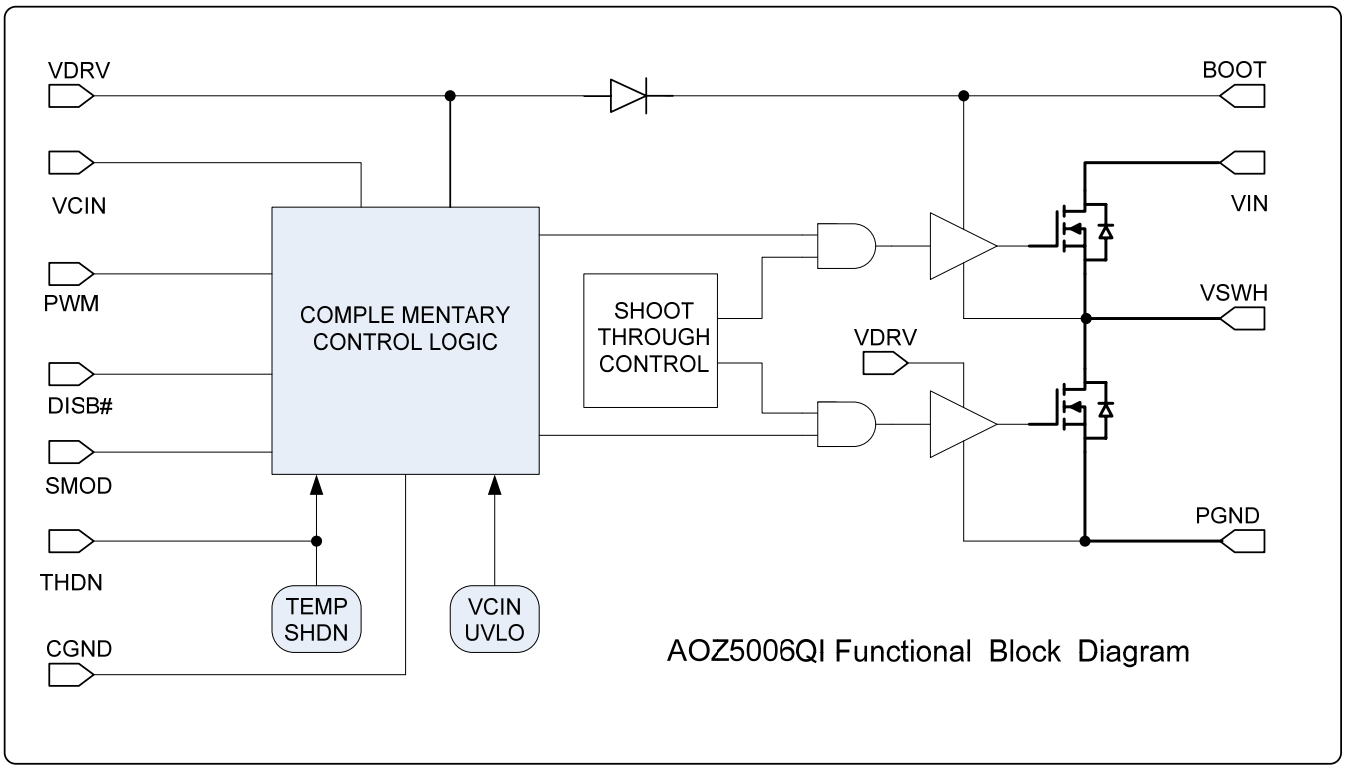

Fig. 2. Functional block diagram

While high performance can be achieved the users need to be aware of certain pitfalls while using DrMOS modules. For example each of the three devices has its own thermal pad to dissipate heat, which means that there are three different junction temperatures inside the module. Power delivered by the module will now be limited by the highest Tj of the three, even if the other two are much cooler in comparison. In general it should be noted that DrMOS is a combination of two discrete devices with an unintelligent driver, all of which are optimised for one function only - switching at the highest efficiency. Other than UVLO and a thermal alarm it does not have any monitoring or protection functions built in. The PWM controller should be designed to perform these functions under all possible operating and transient conditions. This article and the next will list some of the other precautions needed while designing with DrMOS modules.

Powering the Module

Basic operating circuit is shown in *Fig 3*. DrMOS modules should be able to work from input voltages of 7V to 16V per Intel specifications. However, most modules including AOZ5006 can work over a wider range of 4.5V to 16V. As with any other synchronous buck converter, large pulse currents at extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply very close to package leads with X7R or X5R quality ceramic capacitors.

An external supply VDRV of 5V is required for driving the MOSFETs. Unlike previous versions, DrMOS Rev 3.0 specifies that the driver shall work with a fixed and narrow supply voltage 5V. This has actually helped the DrMOS manufacturers since MOSFET performance can be better optimised at a specific gate voltage rather than over a wide range. The reduced gate voltage also helps to minimise gate losses at high switching frequencies. Both MOSFETs are designed with low gate thresholds so that switching and drive losses are reduced without compromising the conduction losses. Gate drivers in DrMOS modules are typically capable of supplying several amperes of peak current into the LS FET to achieve extremely fast switching. As with the main power input a bypass capacitor close to device leads is strongly recommended for the driver. The control logic supply VCIN is separate from the drive supply VDRV, but can be derived through an RC filter to bypass the switching noise as shown in *Fig. 3*. VCIN is monitored for UVLO conditions and both outputs are actively held low unless adequate gate supply is available. Outputs can also be turned off through the DISB# pin. When this input is grounded the drivers are disabled and held active low. The module is in standby mode with low quiescent current of less than 60 uA.

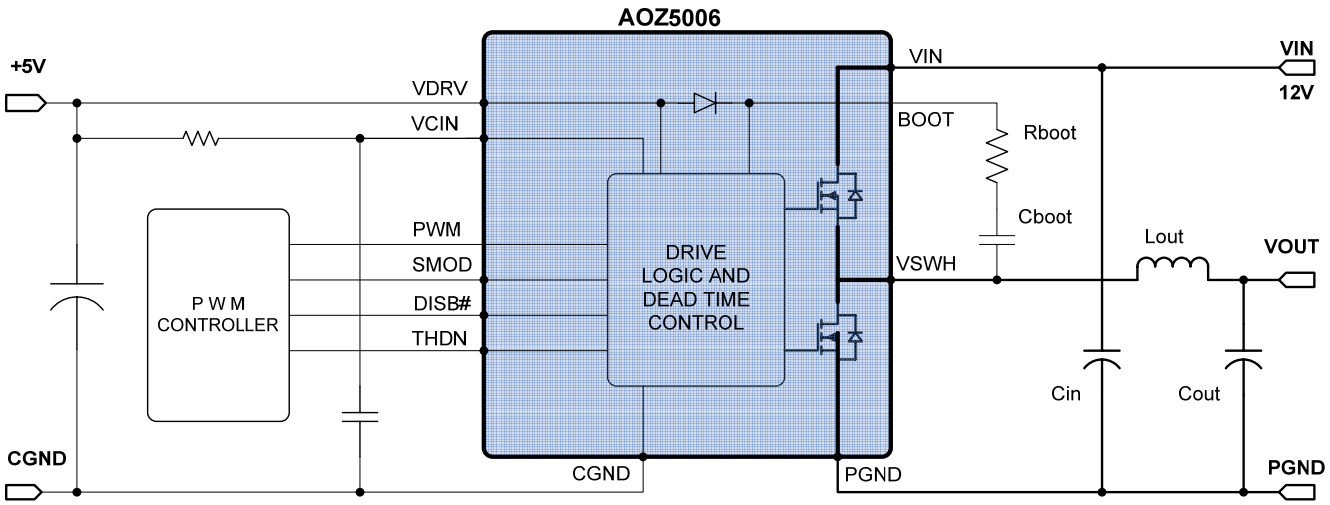

Fig. 3. Powering the DrMOS

PWM Input

As the operating frequencies continue to climb with multi phase topologies, the internal clocks of the PWM ICs have to operate in multi MHz ranges. Many of them have digital interfaces with input signals from 3.3V logic. Alternately the PWM function itself may be realised in a DSP or FPGA rather than a dedicated PWM IC. In such cases the PWM input to the DrMOS module will be compatible with 3.3V rather than 5V. To accommodate different inputs, beginning with Rev 3.0 some DrMOS modules, including AOZ5006, are being offered with two PWM options. AOZ5006QI is intended for use with TTL compatible PWM inputs. AOZ5006QI-01 has lower thresholds on the PWM signal and can operate with 3V inputs. See *Table 1* for typical thresholds for PWM logic as well tri state operations. All other parameters are identical for the two versions. Note that 3.3V/5V levels refer only to PWM input compatibility; both versions run off the same 5V drive and control supply.

While the added flexibility is useful it also calls for extra care by way of matching the right PWM generator with the right version of DrMOS. For example if the 3.3V compatible AOZ5006QI-01 is used with a 5V controller, any PWM level between 1.75 ~ 3.7V will be interpreted as high input by DrMOS. A high impedance PWM signal intended as tri state will actually result in the HS FET being indefinitely turned on. Some DrMOS versions claim to be compatible with both 3.3V and 5V logic inputs which may not hold true in the tri state. The designer needs to check the state and level of PWM output under all possible conditions and make sure that it meets all of DrMOS requirements for the intended operation.

Thresholds –>	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
	V	V	V	V
AOZ5006QI	3.9	1.0	1.3	3.7
AOZ5006QI-01	2.0	1.0	1.3	1.75

Table 1. PWM Input and tri state thresholds

Typical timing diagram between PWM input and gate driver outputs is shown in *Fig. 4*. The PWM is also a tri state compatible input. When the input is high impedance or unconnected both gate drives will be off and the gates are held active low. There is a hold off delay between the time PWM signal enters tri state window and the corresponding gate drive is pulled low. This delay is typically 160 nS and intended to prevent spurious triggering of the tri state mode which may be caused either by noise induced glitches in the PWM waveform or slow rise and fall times.

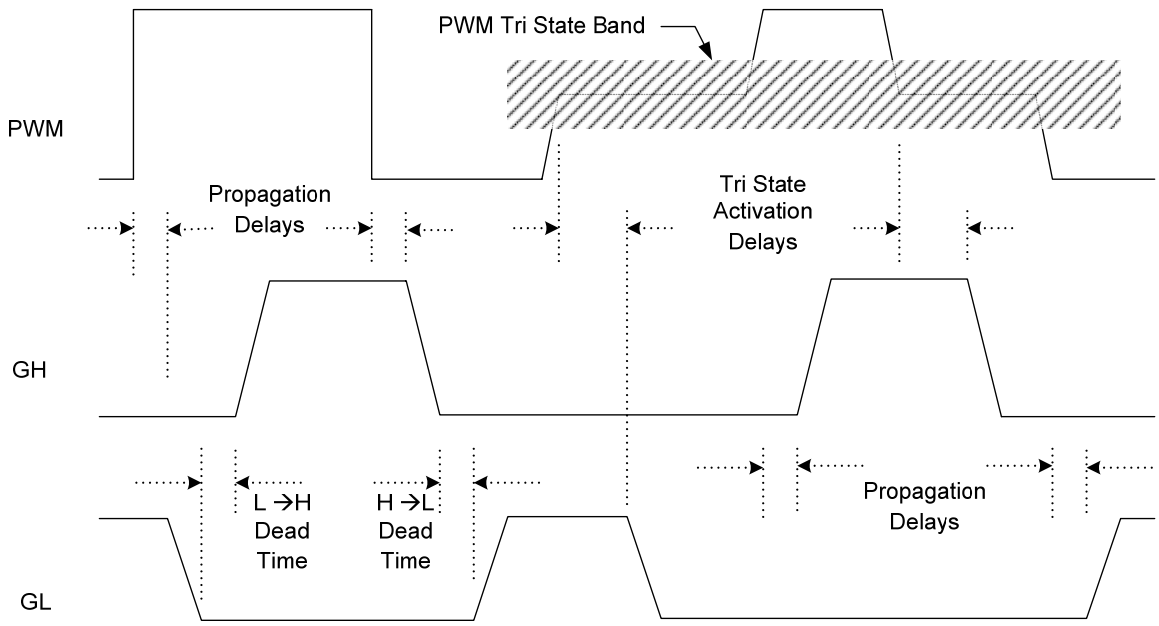

Fig. 4. Timing diagram

Diode Mode Emulation of Low Side MOSFET (SMOD)

DrMOS modules can be operated in diode emulation or Skip Mode using the SMOD pin. This is useful if the converter has to operate in asynchronous mode during start up, light load or under pre bias conditions. If SMOD is taken high, the driver will follow the PWM signal and generate both high and low side complementary gate drive outputs with minimal delays necessary to avoid cross conduction. When the pin is taken low, HS FET drive is not affected but diode emulation mode is activated for the LS FET. The exact implementation of diode emulation mode varies among manufacturers. See *Table 2* for a comprehensive view of all logic inputs and corresponding drive conditions.

Care must be exercised while using the SMOD function, particularly if PWM and SMOD signals originate from different sources in the system. Diode emulation must be disabled and normal synchronous operation must be resumed if the load current is more than the "light" levels. Failure to do so will impair the efficiency and may result in failure of the device due to excessive losses. If the PWM controller implements current sharing/limiting by sensing the drop across LS FET during off time, the diode mode will interfere with that operation and may not be usable at all.

DISB#	SMOD	PWM	GH	GL
L	X	X	L	L
H	L	H	H	L
H	L	L	L	SMOD
H	H	TRI STATE	L	L
H	H	H	H	L
H	H	L	L	H

Table 2. Control logic truth table

Gate Drives

DrMOS modules integrate high speed drivers that generate a level shifted gate drive for the HS FET and a complementary drive for the LS FET. Multi layered, adaptive timing schemes are implemented to minimise propagation delays, dead times and, at the same time, avoid cross conduction. When the PWM signal makes a transition from H → L or L → H, the corresponding gate drive GH or GL begins to turn off. The adaptive timing circuit monitors the falling edge of the gate voltage and when the level goes below 1V, the complementary gate driver is turned on. The dead time between the two switches is minimised, reducing the diode conduction losses. The adaptive circuit also monitors the switching node VSWH and ensures that transition from one MOSFET to another always takes place without cross conduction even under transient and abnormal conditions of operation.

Gate contacts GH and GL are brought out on pins 6 and 36 respectively. However these connections may not be made directly to MOSFET gate pads and their voltage measurement may not reflect the actual gate voltage applied inside the package. The gate contacts are primarily for functional tests during manufacturing and no connections should be made to them in the application.

Thermal Alarm

AOZ5006 series of DrMOS modules offer temperature sensing and alarm according to Rev 3.0 Intel specifications. This is an optional requirement and may not be available in all DrMOS brands. THDN is an open drain pin that is pulled to CGND when the junction temperature exceeds 150 ^{O}C. The flag is reset when the temperature cools down to 135 ^{O}C. By necessity the driver pad temperature is sensed, not on any of the MOSFETs. Note that THDN pin is only an alarm and does not provide any shutdown. In the system, power shutdown is a planned and sequentially executed event and cannot be done by the MOSFET driver.

References:

1) http://www.aosmd.com/pdfs/datasheet/AOZ5006QI.pdf
2) http://www.intel.com/assets/pdf/refmanual/drmos.pdf
3) “Driver & MOSFETs Module (DrMOS) for Desktop/Server Applications Rev 3.0” Intel Specification